

EXPRESS MAIL NO.: EL 477 033 757 US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of: Fukutomi et al.

Group Art Unit: to be assigned

Serial No.: to be assigned
(Continuation of 10/008,616)

Examiner: to be assigned

Attorney Docket No.: 7426-082

Filed: concurrently filed

New York, NY
January 8, 2002

For: FABRICATION PROCESS OF
SEMICONDUCTOR PACKAGE AND
SEMICONDUCTOR PACKAGE

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Applicants respectfully request entry of the following amendment and
remarks in to the file of the above identified application.

IN THE CLAIMS:

Please cancel claims 1-13.

Please add the following new claims:

14. (New) A method of producing a substrate for mounting semiconductor
devices thereon, said substrate having an insulating supporting member and plural
sets of wiring, comprising the steps of:

1004408-010800

forming plural sets of a semiconductor device mounting region and a resin-sealing semiconductor package region outside of said semiconductor device mounting region on a surface of said insulating supporting member;

forming said plural sets of wiring with a predetermined wiring pattern including wire-bonding terminals, external connecting terminals and the wirings that connect said wire-bonding terminals with said external connecting terminals,

wherein in the wiring forming step, said wiring is formed in a manner that said semiconductor device mounting region and said semiconductor packaging region are arranged repeatedly in plural numbers in a row and a column respectively with the same predetermined wiring pattern.

15. (New) The method of producing a substrate for mounting semiconductor devices thereon according to claim 14, wherein in said step of forming said plural sets of wiring, there are provided plural number of blocks of said wiring formed in a manner that said semiconductor device mounting region and said semiconductor packaging region are arranged repeatedly in plural numbers in a row and a column respectively with the same predetermined wiring pattern.

16. (New) The method of producing a substrate for mounting semiconductor devices thereon according to claim 14, wherein said wire-bonding terminal is formed in said semiconductor package region and said method further comprises the step of plating nickel and gold on a surface of said wire-bonding terminal.

17. (New) The method of producing a substrate for mounting semiconductor devices thereon according to claim 14, wherein said external connecting terminals are exposed on a surface of said insulating supporting member, on an opposite side of which said semiconductor device is mounted, and are arranged in a grid pattern at positions corresponding to said semiconductor device mounting region and said semiconductor packaging region.

18. (New) The method of producing a substrate for mounting semiconductor devices thereon according to claim 14, wherein said wiring is formed on one surface of said insulating supporting member, and said method further comprising the step of forming openings in said external connecting terminals in said insulating support member.

19. (New) The method of producing a substrate for mounting semiconductor devices thereon according to claim 18, wherein said openings are formed at least by any of stamping, drilling, laser beam matching and wet etching.

20. (New) The method of producing a substrate for mounting semiconductor devices thereon according to claim 14, wherein said insulating supporting member comprises an adhesive layer on its surface,

said method further comprises, after the step of forming said openings, the steps of bonding said insulating supporting member and a piece of metallic foil via said adhesive layer, and

in the step of forming said plural sets of wiring, said wiring is formed by etching said piece of metallic foil thus bonded.

21. (New) The method of producing a substrate for mounting semiconductor devices thereon according to claim 14, wherein said insulating supporting member comprises a piece of metallic foil on its surface and wherein in the step of forming said plural sets of wiring, said wiring is formed by etching said piece of metallic foil.

22. (New) A substrate for mounting semiconductor device thereon having an insulating supporting member and plural sets of wirings, comprising plural sets of a semiconductor device mounting region and a resin-sealing semiconductor package region outside of said semiconductor device mounting region, wherein

said wirings comprises a predetermined wiring pattern including wire bonding terminals and external connecting terminals and wirings that connect said wire bonding terminals and said external connecting terminals, and

said semiconductor device mounting region and said semiconductor packaging region are arranged repeatedly in plural numbers in a row and a column respectively with the same wiring pattern.

23. (New) The substrate for mounting a semiconductor device thereon according to claim 22, wherein there are provided plural number of blocks of said wirings formed in a manner that said semiconductor device mounting region and

said semiconductor packaging region are arranged repeatedly in plural numbers in a row and a column respectively with the same wiring pattern.

24. (New) The substrate for mounting semiconductor devices thereon according to claim 22, wherein said wire-bonding terminal is formed in said semiconductor packaging region, and said wire-bonding terminals comprises a nickel and gold plate layer on its surface.

25. (New) The substrate for mounting semiconductor devices thereon according to claim 22, wherein said external connecting terminals are exposed on a surface of said insulating supporting member, on opposite side of which said semiconductor device is mounted, and are arranged in a grid pattern at positions corresponding to said semiconductor device mounting region and said semiconductor packaging region.

26. (New) The substrate for mounting semiconductor devices thereon according to claim 22, wherein said wiring is formed on one side of said insulating supporting member, and openings are provided at portions of said external connecting terminals of said insulating support member.

27. (New) The method of producing a semiconductor package comprising the steps of:

mounting a semiconductor device on each of said plural semiconductor devices mounting regions of the substrate for mounting semiconductor device thereon according to claim 22 by employing a die bonding material;

electrically connecting said semiconductor device with said wire-bonding terminal by wire-bonding;

sealing said semiconductor package region including said plural semiconductor devices with a sealing resin connected in one-piece;

forming solder bumps on said external connection terminals; and

cutting said substrate for mounting semiconductor devices thereon and said sealing resin in one operation to be separated into the individual semiconductor package.

28. (New) The method of producing a semiconductor package according to claim 27, wherein said die-bonding material is a die-bonding film.

29. (New) The method of producing a semiconductor package according to claim 27, wherein said die-bonding material is a die-bonding tape.

30. (New) The method of producing a semiconductor package according to claim 27, wherein said cutting is carried out by dicing work.

31. (New) The semiconductor package produced by a method according to claim 27.


REMARKS

Claims 14-31 are in the case. Claims 1-13 have been canceled.

No fee is believed to be due for this amendment. Should any fee be required, please charge such fee to Pennie & Edmonds LLP Deposit Account No. 16-1150.

Respectfully submitted,

Date January 8, 2002



Charles E. Miller 24,576
(Reg. No.)

PENNIE & EDMONDS LLP
1155 Avenue of the Americas
New York, N.Y. 10036-2711
(212) 790-9090

10042403 010302